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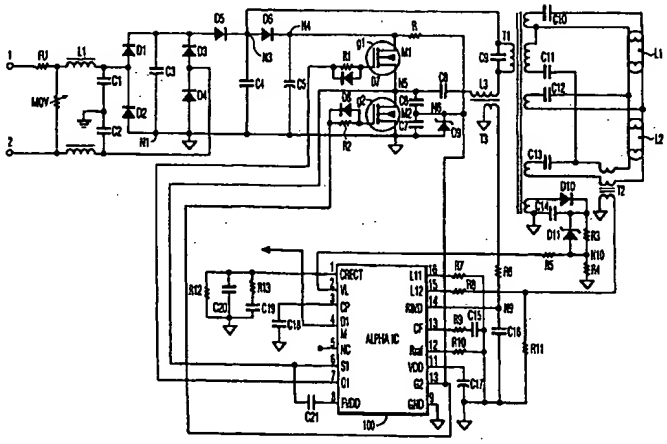

(57) Abstract

A high frequency dimmable electronic ballast comprising a single stage feedback inverter and power factor controller which regulates the power delivered to a load by the inverter at low dim levels such that sufficient lamp crest factor is maintained for load changes from 100 % to 10 %. Sufficient load current crest factors are obtained for variable load (dimming) by operating the ballast in a closed loop configuration, whereby the average value of the load current and/or power is measured and regulated. In one aspect of the present invention, an electronic ballast comprises a single stage feedback inverter for supplying high frequency power to a load in response to driving signals; current sensing means for sensing current flowing in the load due to the supplied load power; voltage detection means for detecting a peak voltage of said load due to the supplied load power; dimming means for generating an illumination signal corresponding to a desired power level of the load; and a controller connected to the single stage feedback inverter and dimming means, for generating the driving signals to cause the inverter to generate the desired power level to the load, whereby the controller processes the sensed load current and the detected peak load voltage to maintain a sufficient lamp crest factor at the desired load power level.

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# DIMMABLE ELECTRONIC BALLAST WITH SINGLE STAGE FEEDBACK INVERTER

The present application relates generally to electronic ballasts and, in particular, to a dimmable electronic ballast with a single stage feedback power factor controller inverter which provides high input power factor and good load current crest factor for variable load dimming.

Typically, a conventional electronic ballast includes a high frequency inverter which operates at a frequency high enough such that component size may be minimized and lamp performance improved. In general, electronic ballasts designed to operate with commercial and residential AC power typically include a full wave rectifier, an DC energy storage capacitor which supplies the inverter, and a resonance circuit for coupling the inverter to the load (e.g., fluorescent lamps). These conventional electronic ballast circuits also include a preconditioner circuit which serves several functions. For instance, the preconditioner circuit operates by boosting the rectified peak AC voltage output from the rectifier and providing a substantially constant DC voltage supply (via the DC storage capacitor) to the inverter.

A continuing goal in the field of electronic ballasts is the desire to design smaller, more efficient and less costly electronic ballasts, while concurrently providing the required minimum harmonic distortion. Recently, one way this goal has been achieved is the implementation of a single stage feedback inverter circuit which allows the preconditioner circuit to be eliminated from the electronic ballast. In these circuits, feedback connections are provided from the high frequency resonant circuit to a node between the rectifier and an isolating diode through which current to an energy storage capacitor flows.

For example, U.S. Patent No. 5,404,082 to Hernandez et al. entitled "High Frequency Inverter with Power-Line-Controlled Frequency Modulation" discloses a low-cost electronic ballast for use with fluorescent lamps which utilizes a single stage feedback inverter topology. The electronic ballast includes a high frequency inverter connected to a storage capacitor which is isolated from the rectifier. The resonant circuit, which supplies current to the lamps, is coupled from the inverter to a node between the storage capacitor and the output of the rectifier. A feedback capacitor in the resonant circuit alternatively receives power from

the rectifier and delivers power to the storage capacitor at the high frequency rate. The inverter frequency is varied during each half cycle of the low frequency input in a direction opposite to the rectified voltage, to minimize the lamp crest factor.

Typically, it is desirable to operate electronic ballasts having single stage feedback inverter topologies at variable load powers, while maintaining requisite lamp crest factors. Due to the open loop operation (i.e., no feedback control of power consumption by lamp loads) of the Hernandez ballast, however, it is not possible to maintain low lamp crest factors during load changes from 100% to 10%. Therefore, there is a need for providing variable load dimming in an electronic ballast having a single stage feedback inverter topology with closed loop control to maintain sufficient lamp crest factor during variable dimming.

The present invention is directed to a high frequency dimmable electronic ballast with a single stage feedback power factor controller inverter, which provides regulation of power delivered to a load at low dim levels such that sufficient lamp crest factor is maintained for load changes from 100% to 10%. Sufficient load current crest factors for variable load (dimming) is obtained by operating the ballast in a closed loop configuration, whereby the average value of the load current and/or power is measured and regulated.

In one aspect of the present invention, an electronic ballast comprises:

a single stage feedback inverter for supplying high frequency power to a load in response to driving signals;

current sensing means for sensing current flowing in the load due to the supplied load power;

dimming means for generating a illumination signal corresponding to a desired power level of the load; and

a controller, operatively connected to the single stage feedback inverter and dimming means, for generating the driving signals to cause the inverter to supply the desired power level to the load, whereby the controller processes the sensed load current to maintain a sufficient lamp crest factor at the desired load power level.

These and other aspects, features and advantages of the present invention will become apparent from the following detailed description of preferred embodiments, which is to be read in connection with the accompanying drawings.

In the drawings,

Fig. 1 is a block diagram of an electronic ballast according to an embodiment of the present invention;

Fig. 2 is a detailed circuit diagram of an electronic ballast shown in Fig. 1 according to an embodiment of the present invention; and

Figs 3a, 3b and 3c are diagrams of test results of the circuit shown in Fig. 2 which illustrate the lamp crest factors obtained at various dimming levels.

Referring now to FIG. 1, a block diagram illustrates the basic components of an electronic ballast in accordance with the present invention. The single stage feedback inverter topology of the electronic ballast includes an alternating current source 10 (e.g., standard AC line voltage of 120 volt and a frequency of 60 hz) provides input power for operating the ballast. An electromagnetic interference (EMI) filter 12 filters high frequency signals and rf noise (e.g., harmonics) generated by the ballast, thereby preventing the conduction of such noise to the AC input source. An AC rectifier circuit 14 rectifies the input AC power to provide rectified DC power. The rectified DC power is coupled via a DC coupler 16 to a DC energy storage device 18 (e.g., an electrolytic capacitor). The DC energy storage device 18 maintains a DC voltage which is relatively higher than the peak of the rectified AC voltage output by the rectifier 14.

An inverter 20 converts the DC voltage stored in the DC storage device 18 to a high frequency voltage having a frequency which may vary between about 20Khz and 75Khz. A resonance circuit 22, operatively connected to the inverter 20, is arranged to resonate at a frequency somewhat lower than the normal range of the high frequency voltage during steady state operation of the ballast. A load 24 (e.g. a fluorescent lamp) is operatively connected to the resonant circuit 22. A feedback loop connects the resonant circuit 22 to a feedback node in the DC coupling circuit 16. During a portion of every high frequency cycle of the inverter 20, current is drawn from the rectifier 14. In addition, during another portion of the high frequency cycle, charging current flows to the DC storage device 18. During the entire cycle of the input AC voltage, DC energy stored in DC storage device 18 is greater than the peak voltage of the rectified AC voltage from the rectifier 14. The operation of the above described single stage feedback inverter circuit is well known in the art. A detailed discussion of its operation can be found, for example, in U.S. Patent No. 5,404,082 to Hernandez et al. entitled "High Frequency Inverter With Power-Line-Controlled Frequency Modulation" and U.S. Patent No. 5,410,221 to Mattas et al. entitled "Lamp Ballast With Frequency Modulated Lamp Frequency," the disclosures of which are incorporated herein by reference.

In accordance with the present invention, the closed loop control circuitry for regulating the power consumed by the load during variable load dimming includes a peak voltage detector 28 for detecting the peak output voltage of the load. A load current sensor 30

senses the current flowing through the load. A driver/controller 32, operatively connected to the peak voltage detector 28 and the load current sensor 30, receives signals from the peak voltage detector 28 and load current sensor to determine the load power. The driver/controller 32 regulates the load power in accordance with dimming level signals provided by a dimming interface 34. In particular, the lamp illumination level can be increased and decreased by decreasing and increasing the frequency of the square wave voltage waveform, respectively. To regulate the load power during variable load dimming so as to obtain the necessary lamp crest factor, the driver/controller 32 adjusts the high frequency waveform generated by the inverter to provide the proper load voltage.

A resonant current sensor 26, operatively connected to the driver/controller circuit 32, provides signals which reflect the amount of current flowing in the resonant circuit 22, whereby the controller 32 processes such signal and adjusts the frequency of the inverter 20 to ensure that the inverter is operating in an inductive mode. The drive control circuit 32 is implemented as an integrated chip which is disclosed in U.S. Patent No. 5,742,134 to Wacyk et al. entitled "Inverter Driving Scheme", the disclosure of which is incorporated herein by reference.

The electronic ballast of the present invention which implements the drive controller disclosed in Wacyk with the conventional single stage feedback inverter will now be discussed in further detail. Referring now to Fig. 2, a detailed circuit diagram of the electronic ballast of Fig. 1 is shown. The source of power for the ballast is an AC power line which is connected to input terminals 1 and 2. The input terminals 1 and 2 are connected to a conventional full bridge rectifier consisting of diodes D1 through D4 via an EMI filter comprising line chokes L1 and L2 and capacitors C1, C2 and C3. The negative terminal (node N1) of the rectifier is connected to circuit ground. The positive terminal (node N2) of the rectifier contains the rectified AC voltage Vrec. The voltage Vrec is coupled to node N3 via fast recovery diode D5. Node N3 is the feedback node, i.e., the node at which the feedback loop connects the resonant circuit 22 to the DC coupling/HF rectifier circuit 16 shown in Fig. 1). A fast recovery diode D6 couples the voltage at node N3 to the storage (buffer) capacitor C5, and acts to rectify the high frequency feedback signal from the resonant circuit.

Transistors M1 and M2 (which are N channel Mosfets) form a high frequency half-bridge inverter having an inverter output node N5. The switches M1 and M2 have a pair of gates g1 and g2, respectively. A resistor R and capacitor C17 are electrically connected via node N6 and serially connected between node N4 and ground. A pair of capacitors C6 and C7 are electrically connected at node N6 and serially connected between node N5 and ground. A

Zener diode D9 shunts capacitor C7. Capacitors C6 and C7 operate to decrease the rate of the rise and fall of the voltage at node N5 during operation of the inverter, thereby reducing switching losses and the level of EMI generated by the inverter. The zener diode D9 establishes a pulsating voltage and node N6 which is applied to capacitor C17 to provide the requisite operating current supplied to pin VDD. A DC blocking capacitor C8 and resonant inductor L3 are serially connected between nodes N5 and the primary of load transformer T1. A resonant capacitor C9 is connected across the primary of load transformer T1.

A winding T3 (i.e., the resonant current sensor 26) is magnetically coupled to the resonant inductor L3 to sense at least a portion of the current flowing through the resonant inductor L3. As explained in further detail below, this current is sensed to ensure that the switches operate in zero voltage switching mode (inductive mode) so as to minimize switching losses.

In this circuit, lamp current is directly fed from the inverter output node N5 through the coupling (DC blocking) capacitor C8 and a series resonant circuit formed by choke L3, resonant capacitor C9 and feedback capacitor C4. When diodes D5 and D6 are nonconducting, all the lamp current flows through the feedback capacitor C4.

The load circuit includes a plurality of serially connected lamps L1 and L2. The load also includes capacitors C10, C12 and C13 which operate to provide filament heating during a preheating stage of operation as is known to those skilled in the art. Capacitor C11 prevents DC power from being applied to the lamps, thereby prolonging the life of the lamps. A signal proportional to the load current is magnetically coupled via current transformer T2 (i.e., the load current sensor 30) which is used by integrated circuit IC 100 (as explained in further detail below) for controlling the load power at variable load levels so as to maintain sufficient lamp crest factor.

The IC 100, which includes a plurality of pins, drives and controls the switches M1 and M2 of the inverter. A detailed discussion of the operation of the IC 100 and its internal circuit architecture can be found in the above incorporated U.S. Patent No. 5,742,134 to Wacyk et al. (hereinafter referred to as "Wacyk"), and will not be reiterated herein. Some of the salient features and functionalities of the IC 100 as it relates to the present invention are generally described below.

A pin VDD is connected to node N6 and provides the bias voltage (approximately 12v) for operating the IC 100. A resistor R10 connected between a pin RREF and ground serves to set a reference current within the Alpha IC 100. The reference current is used for, among other things, regulating the minimum inverter frequency. A resistor R9 and

capacitor C15, serially connected between a pin CF and ground, sets the frequency of a current controlled oscillator (CCO) within the IC 100. A capacitor C18 connected between a pin CP is employed for timing of both the preheat cycle and the nonoscillation/standby mode. A GND pin is connected directly to ground. A pin G1 is connected to the gate g1 of switch M1 via a parallel combination of resistor R1 and diode D7. Likewise, a pin G2 is connected to the gate g2 of switch M2 via a parallel combination of resistor R2 and diode D8. A pin S1 is directly connected to node N5 and receives the voltage at the source of switch M1. A pin FVDD is connected to node N5 via a capacitor 21 and represents the floating voltage of IC 100 (capacitor 21 provides energy to the upper gate switch driver M1).

A pin RIND is electrically coupled to a node N9 which serially connects resistor R6 and capacitor C18 between winding T3 and ground. The input voltage at pin RIND is a representative measure of the current level flowing through resonant inductor L3. The current through resonant inductor L3 is measured to determine whether the inverter is in or near a capacitive mode of operation. (i.e., when the current flowing through resonant inductor L3 leads the voltage across switch M1). In near capacitive mode of operation, the current flowing through the resonant inductor L3 is close but does not lead the voltage across switch M1. As discussed in detail in Wacyk, internal inductor current sense circuitry of IC 100, which is operatively connected to pin RIND, detects whether forward conduction or body diode conduction (from the substrate to the drain) of switch M1 or M2 occurs. When the inverter is in capacitive mode or near capacitive mode of operation, the inductor current sense circuitry causes the inverter frequency to rise quickly, so as to ensure that the inverter is operating within an inductive mode (i.e., the voltage across switch M2 during its non conductive state is leading in phase over the current flowing through resonant inductor L3). The IC 100 also regulates the amplitude of the current flowing through the resonant inductor L3 by sensing the voltage at Pin RIND.

A pin LI2 is connected to current sensing transformer T2 via resistor R8. A pin LI1 is connected to ground via a resistor R7. The difference in currents flowing in pins LI1 and LI2 is a measure of the sensed current flowing through the load (lamps). This sensed current is processed by the IC 100 to ensure sufficient lamp crest factors are obtained during full load operation and variable dimming (as discussed below).

A pin VL is connected to a network consisting of a parallel connection of diode D10 and capacitor C14, and detects the peak load voltage applied to the lamps (via a portion of the secondary winding of transformer T1). The VL pin is used, *inter alia*, for regulating lamp power and protecting the lamp load from overvoltage conditions. The current input into

the VL pin is proportional to the peak lamp voltage (i.e., a current flowing in resistor R5 due to the scaled voltage at node N10). The current flowing into pin VL is multiplied by internal circuitry with the differential current between pins LI1 and LI2, to produce a rectified AC signal representing the product of the lamp current and the lamp voltage which is used for regulating the power of the load. For deep dimming levels (load levels of 15% or lower), it is preferable to regulate the load power using the peak load voltage and load current measurements. It is to be understood, however, that for higher dimming levels (greater than 15%), load power regulation may be significantly achieved by processing the sensed load current.

The rectified AC current flows out of a pin CRECT into ground via a parallel connection of resistor R12, capacitor C20 and a series connection of resistor R13 and capacitor C19, whereby the AC current is converted to a DC voltage which corresponds to the average power of the load (load voltage times load current).

A DIM pin is connected to a dimming control interface (not shown). The voltage applied to the DIM pin corresponds to the level of illumination as set by dimming control interface (the voltage at the DIM pin is a DC voltage). The desired illumination level of the lamps L1 and L2 is set by the voltage at the DIM pin. The voltage at the CRECT Pin is forced equal to the voltage at the DIM pin by a feedback circuit within the IC 100. The feedback loop includes a lamp voltage sensing circuit (i.e., the peak detection circuit discussed above and the VL pin as well as the internal circuitry of IC 100 operatively associated with pin VL) and a lamp current sensing circuit (i.e., the transformer T2 and the LI2 pin as well as the internal circuitry of IC 100 operatively associated with pins LI1 and LI2). The inverter switching frequency is adjusted based on this feedback loop whereby the CRECT pin voltage is made equal to the voltage at the DIM pin. The CRECT voltage varies between .3 and 3.0 volts and the IC 100 clamps the voltage at Dim pin to .3 and 3.0 v. It is to be appreciated that the signal provided at the DIM pin may be provided through different methods known by those skilled in the art such as phase angle dimming in which a portion of the phase of the AC input line voltage is cut off. Such methods convert the cutoff phase angle of the input line voltage into a DC signal applied to the DIM pin.

Initially, when the lamps ignite, the voltage at the CRECT pin is zero. As the current of the lamps increases, the current flowing from the CRECT pin (which is proportional to the product of the lamp voltage and lamp current) charges capacitor C20. The switching frequency of the inverter will decrease or increase until the voltage at the CRECT pin is equal

to the voltage at the DIM pin. In general, a voltage of .3 volts is equal to 10% of full load output and a voltage of 3 v. corresponds to full (100%) light output).

Advantageously, by implementing the above IC controller 100 with the conventional single stage feedback inverter topology, sufficient lamp crest factor can be maintained when operating the electronic ballast under variable load conditions. Referring to Figs. 3a, 3b, and 3c, test results of the circuit of Fig. 2 illustrate that sufficient lamp crest factor is obtained for variable loads. For instance, Fig. 3a shows a lamp crest factor of not more than 1.6 is obtained for load current at 100% (no dimming). Fig. 3b shows a lamp crest factor of not more than 1.8 is obtained with load current at 50%. Fig. 3c. shows a lamp crest factor of not more than 2.0 is obtained with load current at 10%.

Although the illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present apparatus and method is not limited to those precise embodiments, and that various other changes and modifications may be affected therein by one skilled in the art without departing from the scope or spirit of the invention. All such changes and modifications are intended to be included within the scope of the invention as defined by the appended claims.

CLAIMS:

1. An electronic ballast, comprising:
a single stage feedback inverter power circuit (14, 16, 18, 20, 22) for supplying high frequency power to a load (24) in response to driving signals;
current sensing means (30, T2) for sensing current flowing in the load due to the supplied load power and for generating a current signal that represents the load current;
dimming means (34) for generating an illumination signal corresponding to a desired power level of the load; and
a controller (32, 100), operatively connected to the single stage feedback inverter, the dimming means and the current sensing means, for generating the driving signals in dependency of the current signal and the illumination signal to cause the inverter to generate the desired power level to the load.

2. The electronic ballast of claim 1, further including voltage detection means (28) for detecting a peak voltage of said load, wherein the controller generates the driving signals in dependency of a power signal that is proportional to the product of the current signal and the detected peak voltage and in dependency of the illumination signal.

3. The electronic ballast of claim 1, wherein said load current sensing means includes a transformer (T2) for magnetically coupling voltage from the load and a resistor network (R8, R11), connected to the transformer, for providing the current signal to the controller.

4. The electronic ballast of claim 1, further including means (Pin RIND) for sensing if said inverter is operating in one of a capacitive mode and a near capacitive mode, wherein said controller provides suitable driving signals to cause a change in the frequency of the inverter that results in an inductive mode of operation.

5. The electronic ballast of claim 1, wherein said single stage feedback inverter circuit comprises:

an input means (1, 2) for connecting to an AC power source;
a full-wave rectifier (14, D1, D2, D3, D4) for rectifying the input AC power;
a DC coupling circuit (16, D5, D6, C4) having a feedback point (N3) associated therewith;
a DC energy storage device (18, C5), operatively connected to the full-wave rectifier via the DC coupling circuit, for storing the rectified AC power;
a half-bridge inverter circuit (20, M1, M2) connected to the DC energy storage device for providing high frequency power at an inverter frequency determined by the driving signals from the controller;
a resonance circuit(22, L3, C9), operatively connecting the half-bridge inverter to the load, comprising at least one resonant inductor (L3) and one feedback capacitor (C9); and
feedback connection means, operatively connecting the resonant circuit to the feedback node of the DC coupling circuit, for providing high frequency power to the energy storage device.

6. The electronic ballast of claim 5, wherein the DC coupling circuit comprises a first diode (D5) connected between said rectifier and said feedback node; and a second diode (D6) connected between said feedback node and said DC storage device, wherein said resonant feedback capacitor (C9) is connected between said feedback node and the resonant inductor (L3).

7. A method for controlling power in an electronic ballast, comprising the steps of:
supplying high frequency power to at least one fluorescent lamp (L2) by a single stage feedback inverter (14, 16, 18, 20, 22);
sensing at least a portion of the current flowing in the load as a result of the supplied power;
processing the sensed load current by a controller (32);
generating driving signals by the controller in accordance with the sensed load current signals for adjusting the high frequency power delivered by the single stage feedback inverter circuit to the load such that a sufficient lamp crest factor is obtained.

8. The method of claim 7, further comprising the steps of: supplying an illumination level signal to the controller; generating driving signals by the controller to adjust the power delivered to the load in response to the illumination level signal.

9. The method of claim 7, further including the steps of sensing the peak load voltage and processing the sensed peak voltage together with the sensed load current to determine the load power.

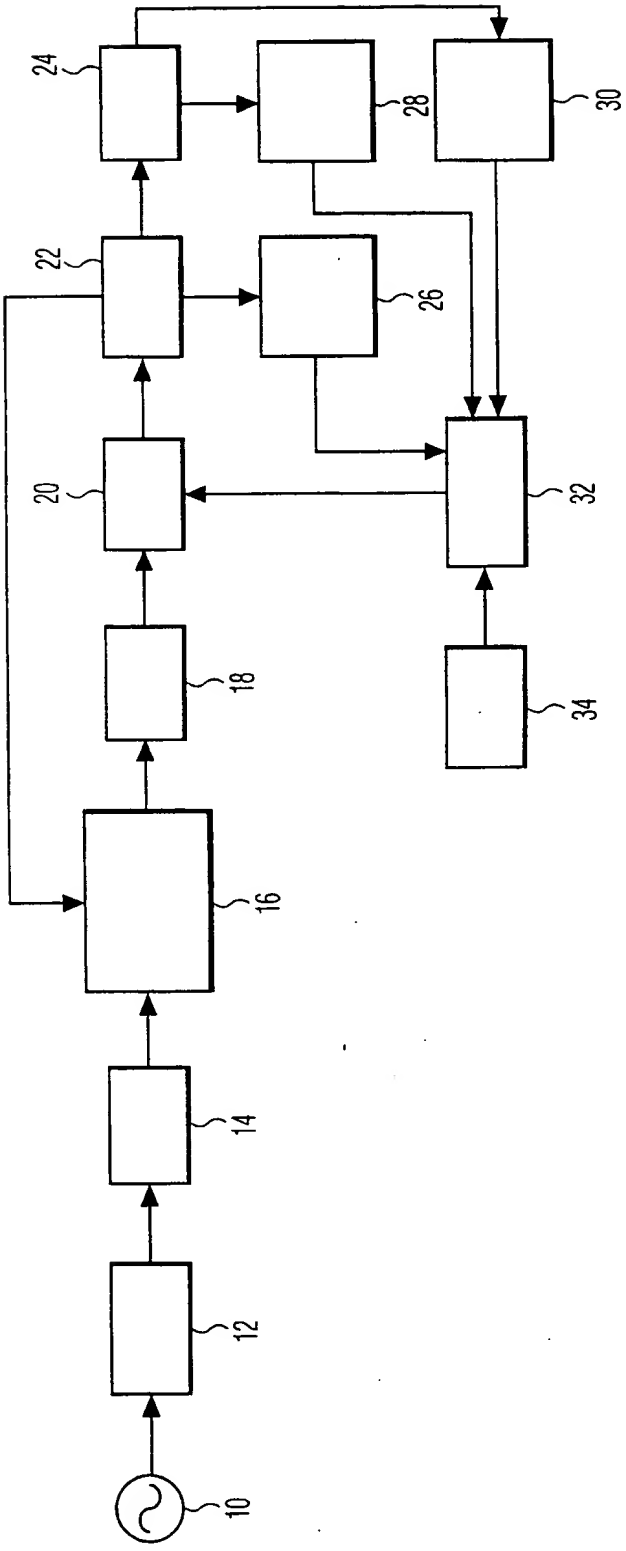
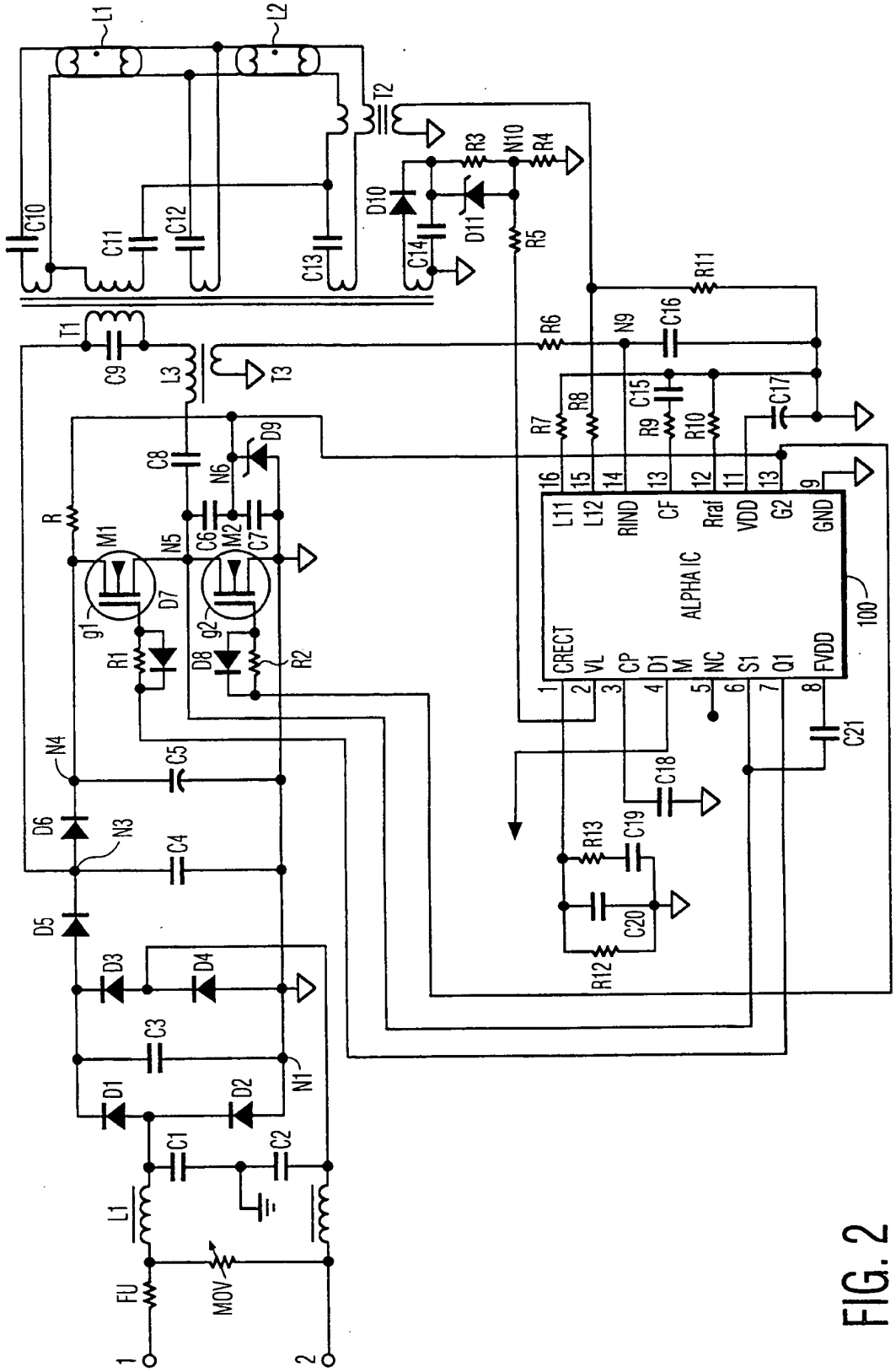



FIG. 1


L1
L2
T2
R3
N10
R4
D10
D11
R5
C10
C11
C12
C13
C14
T1
C9
L3
T3
R6
N9
C16
R11
R7
R8
C15
R9
R10
C17
C8
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C1
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L1
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L12
RIND
CF
Rraf
VDD
G2
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C21
C18
R13
C19
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R12

FIG. 2

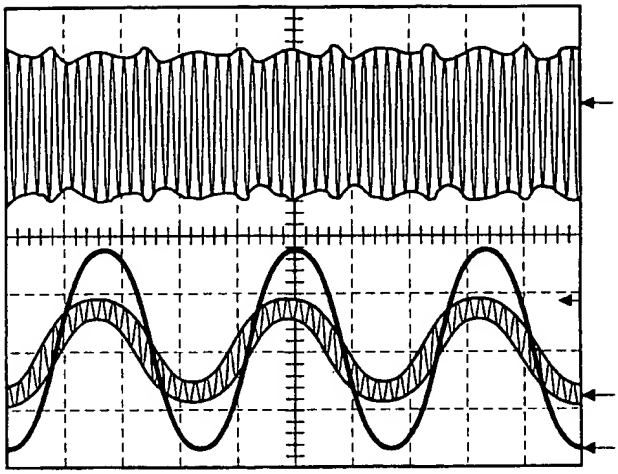

FIG. 3a

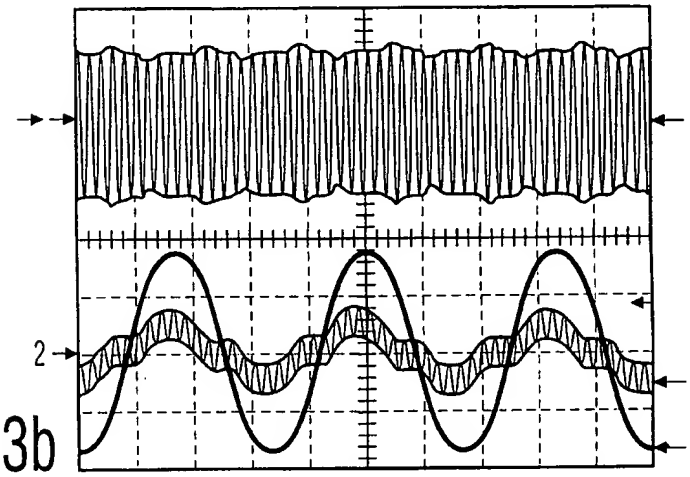


FIG. 3b

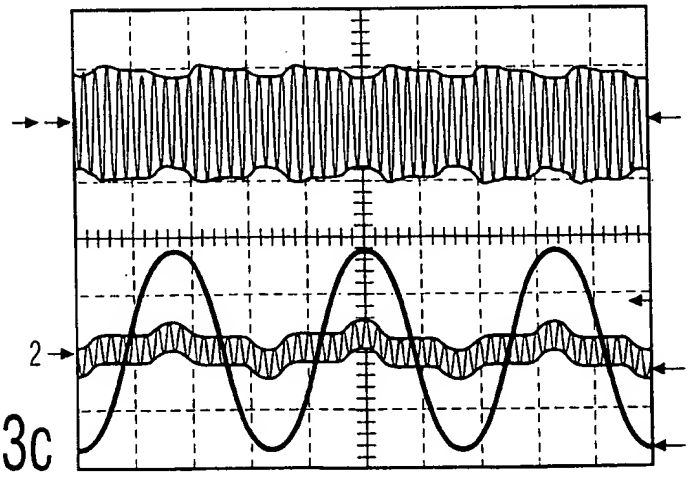


FIG. 3c

# INTERNATIONAL SEARCH REPORT

Inter . xnal Application No
PCT/EP 99/10195

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05B41/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | US 5 742 134 A (WACYK IHOR T ET AL)<br>21 April 1998 (1998-04-21)<br>cited in the application<br>the whole document | 1-9 |
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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2

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